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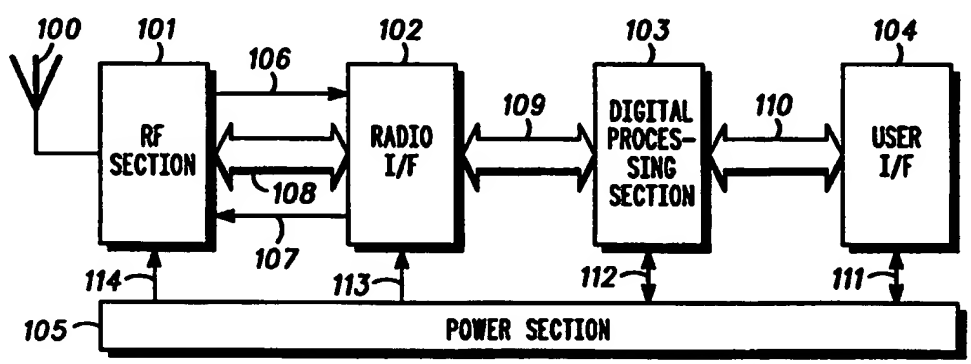

(57) Abstract

A communications terminal adapts to different operating standards by using software algorithms and digital processing instead of physically dedicated hardware. The communications terminal includes digital processing circuits (103) having a digital signal processor and microprocessor circuits, volatile and non-volatile memory, signal characteristics stored in memory and receiver circuitry to receive and digitize a radio signal. The communications terminal receives the radio signal, converts the radio signal into a digital signal and compares the signal characteristics of the digital signal to signal characteriscs of stored signals. The comparison of the signals identifies the standard of the radio signal and determines the format and protocol of the signal. The hardware is then reconfigured to operate according to the identified standard, format and protocol.

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SELF CONFIGURING MULTI-MODE COMMUNICATIONS TERMINAL

Field of the Invention

This invention relates generally to improvements in cellular telephone communications. More particularly, the present invention allows a communications terminal to adapt itself to its environment without having to incorporate multiple physical transmission facilities, with their association to different standards having different formats and protocols. A single hardware implementation is automatically reprogrammed, by using software algorithm and digital processing, in response to the detected characteristics of a received signal indicating the protocol and format to be used.

Background of the Invention

The proliferation of incompatible standards for wireless communications has forced many users to buy or lease multiple terminals, each one capable of operating according to a specific standard. The problem of using standard specific terminals is particularly difficult for international mobile users, who encounter different systems at different times. Nowhere is the problem more acute than in the area of cellular telephony, where Advanced Mobile Phone Service (AMPS), Narrow Advanced Mobile Phone Service (NAMPS), Time-division Multiple Access (TDMA), Global System for Mobile Communications (GSM), Code-division Multiple Access (CDMA), and other systems compete with different degrees of success in different parts of the world, and even within different countries.

In the cellular telephony area, some systems have a requirement for backward compatibility with earlier systems, so that a mobile terminal for a newer standard must be able to operate also in a system employing the older standard. This "dual mode" capability is expressly stated in IS-136, a specification for TDMA/AMPS mobile systems. The dual mode of

operation has in the past required more hardware than what is needed to implement any one of the standards. The present invention describes a method whereby multiple modes of operation are possible with little or no additional hardware, and where the operational mode is automatically adapted to the standard of the received signal.

Dual or multi-mode telephony or radio operations has been addressed in the past. For example, U.S. Patent No. 5,438,682 to Durtler et al, can change between analog mode and TDMA mode based on the location of the cellular telephone user. However, this approach is concerned with the power of the cellular telephone and dedicated hardware is needed for different standards of the different systems.

There are other dual cellular telephones capable of switching between systems, U.S. Patent No. 5,535,432 to Dent, switches between operating a cellular telephone between land based cellular and orbiting satellite systems and is concerned with a frequency synthesizer which can provide both wide and narrow channel spacing for the different bandwidth of each system. However, Dent cannot adapt to different standards unless all of the parameters of the standards are already stored in the cellular telephone. In addition, Dent relies on implementing two antennas and dedicated hardware.

A system for cellular telephony which can switch in an automatic mode to different standards without having dedicated hardware for each of the formats and protocols of the different standards would overcome the shortcomings of the inventions noted above.

Summary of the Invention

It is therefore an object of the present invention to allow a terminal to operate in conformance with a number of different standards without having to contain multiple, standard specific hardware implementations.

A further object of the invention is to minimize the cost of the terminal by enabling it to conform to a range of both present and future

operational standards without having to contain, at any one time, all the software means to implement all these standards.

A further object of the invention is to allow the terminal to adapt itself automatically to the operational characteristics of the network or link in which it is used.

In most communications networks, there is a direct correspondence between the protocol of the signal in one direction, and the protocol of the signal in the other direction. Protocols for call setup and teardown and other monitor and control functions can in most cases also be deduced if the standard governing the protocol of the received signal can be determined from the characteristics of the signal. Only a small amount of core functionality software is needed in a receiving terminal to be able to identify the standard.

The present invention takes advantage of the limited scope of this core functionality, plus the intelligent processing and analysis of the signal made possible by its digital processing based design, to achieve standard identification with a minimum amount of hardware and software. Once the standard is identified, the full required terminal functionality and operating parameters are known and the proper executable code can be implemented. Due to the implementation of most functions in software or software configurable hardware, the terminal can then configure itself to operate in this mode without having a multiplicity of terminal types implemented in hardware, and without user intervention.

The heavy use of software implementation of functions reduces the number of physical components needed in the terminal and makes possible enhanced performance and reliability of the communications link. The core functionality software also makes it possible to "download" the proper executable code for various present and future standards without requiring a physical change in the terminal. This feature can be used to limit the amount of software code carried locally within the non-volatile memory of the digital processing circuits. The implementing

software can configure the terminal to the degree that it is able to transmit a download request for the appropriate standard, and to receive the download for the proper executable code not carried locally. Such a feature is a considerable asset in systems where many communications link protocols are possible, but a control channel exists with a fixed, known format and protocol.

Brief Description of the Drawings

FIG. 1 is a top level diagram of a communication terminal system.

FIG. 2 is an example of the Radio Frequency Section of a preferred communication terminal system.

FIG. 3 is an example of the Radio Interface of a preferred communication terminal system.

Other objects, features and advantages will occur to those skilled in the art from the following description of a preferred embodiment and the accompanying drawings.

Detailed Description of the Drawings

Referring to FIG. 1, a top level block diagram of the present invention is shown. FIG. 1 shows how the different components of a communication terminal system interrelate. In FIG. 1, the communications terminal is shown to comprise six main functions: antenna 100, Radio Frequency (RF) Section 101 (see FIG. 2 for example embodiment), Radio Interface 102 (see FIG. 3 for example embodiment), Digital Processing Section 103, User Interface 104 and Power Section 105.

The terminal communicates with other terminals and communications nodes by transmitted, modulated radio carriers and received, modulated radio carriers, radiated and received respectively via antenna 100. RF Section 101 handles both transmission and reception of the carrier signals. RF Section 101 generates the transmitted carrier and downconverts and filters the received carrier to an Intermediate

Frequency (IF) signal 106. The modulation of the transmitted carrier is controlled by modulation signal 107, while the frequency and power of the carrier are set by RF control bus 108. RF control bus 108 also controls the timing of the receiver and the signal gain in the receive path.

Radio Interface 102 contains multiple Analog to Digital ("A/D"), Digital to Analog ("D/A") converters and digital control registers. IF signal 106 is digitized for further digital filtering and demodulation by one of these A/D converters. The digitized signal is provided to Digital Processing Section 103 via digital interface bus 109. Modulation Signal 107 and analog signals in RF control bus 108 are generated by D/A converters based on digital inputs from Digital Processing Section 103. Digital control registers in Radio Interface 102 furnish additional, digital control signals for RF control bus 108, while analog monitor signals from RF Section 101 are converted to digital values by additional A/D converters in Radio Interface 102. Therefore, Radio Interface 102 serves as a signal format converting interface between the essentially analog circuits of RF Section 101 and the digital processing and control functions of Digital Processing Section 103. Radio Interface 102 is easily implemented as a single chip, and can even be absorbed into a larger chip, containing major portions of Digital Processing Section 103 and User Interface 104.

Most of the standard specific processing of the transmit and receive signals takes place in Digital Processing Section 103. This processing is entirely digital and is performed via software algorithms. Thus the mode of operation and the operational parameters are easily modified. The modification entails simply selecting a different executable code for the digital processing functions. Various symbol rates, data formats and modulation types can be easily accommodated, if the format of the received signal can be identified and the corresponding executable code selected. In many systems, if the received protocol can be identified, the proper transmit protocol can also be identified. The digital processing circuitry identifies the standard of the received signal by comparing the

characteristics of the received signal with the signal characteristics of at least one set of signal characteristics stored in non-volatile memory. In other embodiments, the terminal may have to select code to correctly filter, demodulate and fully decode the received signal in order to obtain information about the right transmit carrier frequency, protocol and bandwidth. In either case, only a small, common core functionality is needed in the receive processing to identify the communications standard of the received carrier.

User Interface 104 contains at least some of the following items, and possibly additional ones: Keypad (or keyboard), alphanumeric (or CRT) display, LEDs, speaker, microphone, tone transducer. User Interface 104 also contains the electronic circuits to interface these items to Digital Processing Section 103. User Interface 104, typically includes A/D and D/A converters, gain controlled amplifiers, LED drivers and a display driver. In the example embodiment of the present invention, which is a cellular mobile handset, User Interface 104 contains all of these items.

Power Section 105 contains a primary power supply, which may be a battery. It may also contain one or more DC to DC converters to generate regulated voltages equal to the nominal primary supply voltage and/or higher and/or lower than this voltage. In addition, electronic switches are incorporated to turn on and off the various output voltages in response to inputs from either User Interface 104 or Digital Processing Section 103. Power Section 105 outputs provide power to block sections 101 through 104 of FIG. 1.

Referring to FIG. 2, an example embodiment of the RF Section 101 of FIG. 1 is shown. This embodiment illustrates a dual mode cellular telephone mobile handset, operating in the 1,900 MHz band. (IS-137A TDMA at 1,900 MHz, and PCS-1900). Although an 800/1,900 MHz dual band functionality for the AMPS/TDMA dual mode feature is not shown, by adding the proper hardware into RF Section 101, the rest of the

equipment can operate in AMPS mode as well if the corresponding software is added or downloaded.

In FIG. 2, the RF signal to and from the antenna is shown as line 200. The RF energy on this line is band split by duplexer 201. Frequencies in the 1,930 MHz to 1,990 MHz range have a path from lead 200 to lead 220, while frequencies in the 1,850 to 1,910 MHz range have a path from lead 239 to lead 200. Received signals on lead 220 are amplified by Low Noise Amplifier (LNA) 202 before they are applied to receiver Band Pass Filter (BPF) 203.

In the example embodiment, BPF 203 has a center frequency of 1,960 MHz and a bandwidth of +/- 32 MHz which allows frequencies assigned to mobile reception in standards 137A and PCS-1900 to pass through the filter but blocks any residual of the transmit carrier, leaking from lead 239 on the duplexer input to lead 220 on its output. The output of BPF 203 is conducted via lead 222 to mixer 204. A second input to mixer 204 is furnished by lead 227, and consists of a carrier signal produced by Main Synthesizer 208. If BPF 205 has a center frequency of 67.71 MHz, the signal on lead 227 has a frequency somewhere in the range 1,997.75 to 2,057.75 MHz.

The output of mixer 204 contains signals in the frequency bands equal to the sum and the difference of the frequencies of its two inputs. The difference band covers 67.71 MHz, which is where BPF 205 selects a segment of this band, centered at 67.71 MHz. Since the frequency on lead ✓characteristic 227 can be varied, any channel in the mobile reception band can be made to appear at the center frequency of the filter.

BPF 205 has a bandwidth of 180 kHz, sufficient to just pass one channel of the PSC-1900 standard, but much wider than required for the IS-137A TDMA channel. For IS-137A TDMA applications, an interference signal as much as 62 dB stronger than the desired channel may be present 60 kHz away from the desired channel, which is centered in the filter bandwidth. The desired channel is then 62 dB below the interference

level. This fact will be dealt with in the description of the Radio Interface 102.

The output of BPF 205 is amplified by Automatic Gain Control Amplifier (AGC) 206. The gain of AGC 206 is controlled by the voltage level on lead 226. This voltage is the output of a control loop that keeps the peak to peak swing on lead 225 more or less constant even though the amplifier input on lead 224 can have a wide range of signal amplitude. The amplifier maintains good linearity in its signal transfer characteristics over the full 80 dB of gain control range. Lead 225 is the intermediate frequency (IF) output from RF Section 101 to Radio Interface 102 (see FIG. 1).

The signal on lead 227 is generated by Main Synthesizer 208. The tuning of its frequency is achieved by software control via a digital input bus 230. Main Synthesizer 208 is tuneable in steps of 10 kHz. In the TDMA mode, it is actually tuned in steps of 30 kHz, while in the PCS-1900 mode it is tuned in steps of 200 kHz. These numbers reflect the channel spacing in the respective standards.

The accuracy of the tuning of Main Synthesizer 208 is given by the accuracy of the frequency reference on lead 229. That accuracy can be made very high by implementing a control loop via software in Digital Processing Section 103. The control loop applies a fine tuning voltage on lead 228, causing Voltage Control Crystal Oscillator (VCXO) 207 to produce an accurate output frequency.

The output of Main Synthesizer 208 is also applied to mixer 209, which as its other input has a signal from Offset Synthesizer 210. Offset Synthesizer 210 generates a signal at a frequency which, when subtracted by mixer 209 from the frequency of the signal on lead 227, produces an output on lead 232 that is at the frequency of the transmitted channel. Mixer 209 is implemented as a single sideband mixer, reducing substantially the mixer output component that is at a frequency equal to the sum of the two input frequencies. In the example embodiment, Offset

Synthesizer 210 generates a signal with a frequency of 147.75 MHz. This makes the transmitted carrier fall in the 1,850.04 - 1909.92 MHz range as the signal on lead 227 is tuned over the 1,997.79 - 2,057.67 MHz range. The selection of 147.75 MHz for the offset frequency insures that no harmonic of this signal falls in the receive carrier band of 1,930 to 1,990 MHz. For dual band operation, Offset Synthesizer 210 is tuned to 112.71 MHz when the equipment is operated in the 800 MHz band. This again puts harmonics of the signal outside the receive RF band.

Offset Synthesizer 210 is used via Mixer 209 to generate the transmit carrier. The reason that a synthesizer is not used to directly generate a frequency equal to the high powered transmitted carrier is because it would be prone to being "pulled" by the modulation on the carrier. This problem is avoided through the use of a fixed frequency offset and the mixer.

The output of Mixer 209 is applied via lead 232 to I/Q Modulator 211. This quadrature modulator can produce any form of modulation of the carrier on its input lead 232 as a result of manipulation of the voltages on its two analog baseband input leads 233 and 234. An FM signal or quadrature phase-shift keying (QPSK) signal according to standard 137A, or a Gaussian minimum shift keying (GMSK) signal according to the PCS-1900, is generated by I/Q Modulator 211 depending on the characteristics of its baseband inputs. The generation of the GMSK signals is described during the description of the Radio Interface 102.

modulation forms

The output of I/Q Modulator 211 is applied to Voltage Gain Amplifier (VGA) 212. The gain of VGA 212 is controlled by the voltage on lead 236, which is adjusted to set the power of the transmitted carrier. The output of VGA 212 is applied to BPF 213, which allows signals in the 1,850 - 1,910 MHz band to pass through, but blocks the residual 2,140 - 2,200 MHz signal from modulator 211. The residual is due to imperfect single sideband performance of mixer 209.

After amplification and filtering, the modulated transmit carrier is applied to Power Amplifier 214. Virtually complete shutdown of the transmission is achieved by removing the supply voltage to the power amplifier, furnished via lead 240. The magnitude of the signal leaking through Power Amplifier 214 as DC power is removed is minimized further by reducing the gain in VGA 212 to the minimum when no transmit carrier is to be generated. When activated by being given its DC supply voltage, Power Amplifier 214 applies the transmit carrier to duplexer 201, where it is routed to lead 200 and antenna 100. As a result of the band splitting nature of duplexer 201, very little of the transmit carrier appears on lead 220. Thus the hardware is capable of simultaneous transmission and reception as well as power efficient transmit/receive time interleaving.

Referring to FIG. 3, Radio Interface 102, shown as a block in FIG. 1, is illustrated in more detail. The analog 67.71 MHz IF signal from the RF Section 101 comes in on lead 225 to the A/D converter 300. This 10 bit A/D converter performs IF subsampling with a sampling rate, which is eight times the symbol rate in the PCS-1900 mode, and about 89.16 times the symbol rate of the IS-137A TDMA mode. The sampling rate is approximately 2.1667 MHz. The sampling rate is also close to the IF frequency of the desired channel divided by 31.25. The significance of these numbers is explained below.

The output of A/D converter 300 is a 10 bit word which is connected to Digital Complex Down Converter 307 via 10 bit parallel bus 320. A sampling pulse provided on lead 321, provides control of the output of A/D converter 300. The sampling pulse rate is approximately 2.1667 MHz. The digital signal processor of the digital processing circuitry adjusts the phase of the sampling signal to obtain optimal sampling for the PCS-1900 mode. In the TDMA mode, the 2.1667 MHz sampling is allowed to free run. This mechanism is part of the bit timing recovery algorithm performed by Digital Processing Section 103.

The sampling rate of the A/D conversion is 2.1667 MHz while the center of the sampled IF band is at 67.71 MHz. The IF band is 180 kHz wide. Since the IF signal is sampled at much less than the Nyquist rate, a number of aliasing bands are produced in the sampled signal, all 180 kHz wide. These bands have center frequencies at frequency points equal to the IF carrier frequency +/- N times the sampling frequency. The band for N=31 has a center frequency of (67,71 - 31 * 2.1667) MHz, or about 543.333 kHz. Other aliasing signals have frequencies above 1 MHz, and in the downconversion, filtering and decimation process, these are filtered out.

Digital Complex Down Converter 307 uses the sampling rate divided by four to translate the 543.333 kHz carrier to baseband I and Q signals 322 and 323, respectively. The sampling rate divided by four is 541.666 kHz, which is 1.667 kHz lower than the carrier frequency. The I and Q signals are therefore presented to Decimating Low Pass Filter 306 with a 1.667 kHz carrier phase rotation remaining, even though the sample timing is adjusted by Digital Processing Section 103. This is later corrected in Digital Processing Section 103. The I and Q signals still have a sample rate of 2.1667 MHz, and for the TDMA mode, they contain signals from multiple received channels.

Filter characteristics of Decimating Low Pass Filter 306 can be controlled to meet the requirements of different signal standards. In the example embodiment of the present invention, Decimating Low Pass Filter 306 has two built in sets of coefficients: one to fit the PCS-1900 mode of operation, and another to fir the TDMA mode of IS-137A. These are selected automatically by detecting the rate of the Symbol Rate Divided By Four input on Lead 324. In other embodiments, Decimating Low Pass Filter 306, which is an all digital implementation, can have its parameters loaded from Digital Processing Section 103 as needed to achieve a wide range of filter characteristics.

In the PCS-1900 mode, Decimating Low Pass Filter 306 performs a minor amount of filtering, achieving a factor of two decimation. In this

mode, only one carrier is present in the bandwidth of BPF 205 in RF Section 101 (see FIG. 2), which performs the major share of the filtering for the PCS-1900 mode. The four samples per symbol, 1.0833 Msamples per second, 10 bit words for I and Q are each converted to a 10.833 Mbps serial format for the digital signal processing. The digital signal processor uses its serial port frame pulse to delineate the word boundaries.

In the TDMA mode, Decimating Low Pass Filter 306 performs a substantial amount of filtering, and also achieves a synchronization of the 2.1667 MHz primary sampling rate to the 97.2 kHz sampling rate for the filtered channel. The filter is sampling the 24.3 ksymbols per second TDMA carrier at more than 89 times the symbol rate. The filtering provides sufficient attenuation of the adjacent and alternate channels to meet standard IS-137A requirements. The filtered signal is then resampled by clock signal 327, which is at 97.2 kHz, and has a phase controlled by the Digital Processing Section bit timing recovery algorithm. Since 97.2 kHz is not 2.1667 MHz divided by an integer, the resampling is equivalent to about 1.1% of a symbol peak to peak sampling jitter. This amount of jitter has no significant effect on the demodulation performance.

The filter output for the TDMA mode has a 972 kbps serial bit rate for each of the 10 bit I and Q samples, connecting these signals to Digital Processing Section 103 over multi-lead line 325.

The 12 bit D/A converter 301 contains an internal 12 bit register that is written to by Digital Processing Section 103. The content of the register is converted to an analog signal that is used to control the gain of AGC amplifier 206 in RF Section 101 (see FIG. 2). A pulse on lead 327 causes the writing of 12 bits of parallel data.

The 8 bit D/A converter 302 contains an internal 8 bit register that is written to by Digital Processing Section 103. Still inside the D/A converter, the content of the register controls a pulse width modulator (PWM), which is followed by a low pass filter, converting the duty cycle of the

pulses into a corresponding DC level. The DC level is used as an automatic frequency control (AFC) to fine tune VCXO 207 in RF Section 101 (see FIG. 2).

Synthesizer Interface 303 translates the format of its inputs from Digital Processing Section 103 into a serial format used to control Main Synthesizer 208 and Offset Synthesizer 210 in RF Section 101 (see FIG. 2).

The 8 bit PWM D/A converter 304 is identical to 8 bit PWM D/A converter 302. It converts an eight bit word written by Digital Processing Section 103 into an analog DC voltage that is used in RF Section 101 to control the power level of the transmitted carrier.

Dual 8 bit D/A converter 305 contains two internal 8 bit registers that are written to by Digital Processing Section 103. The information for each register is the digitally filtered I and Q transmit signals respectively. The update rate is four per symbol per register. The data arrives in serial form from the serial port of Digital Processing Section 103. After conversion to analog form, the I and Q signals are low pass filtered to remove frequency components arising from the digital word rate before being applied to I/Q modulator 211 in the RF Section 101.

Address Decoding and Timing Generator 308 is connected to Digital Processing Section 103, allowing Digital Processing Section 103 to write to the circuits in Radio Interface 102.

In a preferred embodiment of the invention, Digital Processing Section 103 contains digital processing circuits having a digital signal processor and microprocessor circuits, volatile and nonvolatile memory, core functionality software and at least one set of signal characteristics representing at least one standard. The digital processing circuits implement digital signal processing tasks associated with the modulation and demodulation of the transmit and receive carrier signals. It also controls the functionality of the RF Section 101 and Radio Interface 102 as described above. Some of the core functionality software include functions associated with call processing, band scanning, User Interface 104

and the control of Power Section 105. Most of these functions are well known in the art, and are not the subject of this patent. Therefore, they will not be described in detail. However, some of the functionality included in Digital Processing Section 103 is an inextricable part of the present invention, and is illustrated in the example embodiment. The significant items are: (a)the use of intelligent processing of a received modulated radio signal to identify the standard of transmission as a specific standard among several possible ones and (b)the ability to automatically configure the receiver and transmitter for operation according to the proper format and protocol for the standard associated with the received carrier signal, without having to contain specific hardware, or even the software, for each standard.

In the context of item (a) above, the following hardware description illustrates how the same hardware, without physical modifications, can be used to implement different transmit and receive standards. The terminal receives modulated radio carrier signals, which are then filtered and converted to digital radio signals, digital I and Q data. Digital Processing Section 103 receives the digital radio signal from the Radio Interface 102, tunes Main Synthesizer 208 across the channels until it finds a modulated radio signal. The present invention then attempts to lock the bit/symbol timing recovery loop to the received signal. If it does not succeed in one mode, it reconfigures the Decimating Low Pass Filter 306 and its own digital bit/symbol timing recovery loop for another standard and tries again. In cases where the same symbol rate is used for more than one standard, additional signal analysis algorithms may be incorporated into the core functionality software to distinguish between them. Through the use of just the core functionality software, the standard of the received carrier can be revealed. In addition, the digital processing circuitry can tune Main Synthesizer 208 to find additional signals and can identify their operating standards. In another embodiment, the digital processing circuitry can have different formats and protocols of different operating

systems stored in non-volatile memory and can switch between operating standards.

Standard identification requires a modest amount of resident core functionality software. To fully conform to all operational requirements of a standard requires much more, specifically in the areas of carrier hopping, burst/frame synchronization, transmission protocol, etc. Once the relevant standard is identified, the digital signal circuitry can initiate loading the appropriate executable code from an available source, which may or may not be local, into the volatile memory of the digital processing circuits. This addresses item (b) above.

In another preferred embodiment, albeit not the cellular telephony example embodiment of the present invention, a common system signaling channel is available, having a specific, constant format, even though the traffic channels may be of a variety of formats. In such a system, very little software needs to be resident in the self-configurable communications terminal. A request for executable code for a specific transmissions link standard can be sent via the system signaling channel to a remote central network administration system. The executable code is received via the return path of this channel and the executable code is stored in the non-volatile memory of the digital processing circuits. Only enough memory to hold one executable code at a time is needed in the terminal. However, additional non-volatile memory can be used to store additional executable code. In such a system, considerable freedom exists to modify, upgrade and add to the standards that the terminal can handle, without having to touch the terminal itself.

With more code resident in the terminal, the terminal can use built-in code to conform to a standard specific format for lower level protocols. By selecting the correct executable code and using the standard specific format to request and receive higher level protocol code, the terminal can still handle multiple formats without having to contain resident complete software for all these protocols. In other preferred

embodiments, the higher level software can also be modified, upgraded and added to without having physical access to the terminal. The software can also be upgraded by reconfiguring the non-volatile memory. The example embodiment of the present invention can fall in this category. Downloadable executable code may be provided by a base station, or it may be available at a dial-up database via terminal (cellular handset) autodialing, once the needed code has been identified. The process is the same for both, where the executable code is uploaded from the base station or database, the code is received by the receiving circuitry of the terminal and is stored in the non-volatile memory of the digital processing circuits.

In the most straight forward case, the complete executable code for each standard to which the terminal can conform is contained in built-in, non-volatile memory. The executable code for the relevant standard is accessed and transferred to volatile memory as operating code when the standard has been identified. Even in this case, modification, upgrading and addition is possible by making the non-volatile memory writeable via a download function. By providing manufacturing options for various size Read Only Memory (ROM) or non-volatile memory, the same hardware design can cost effectively be used to make a handset functioning exclusively according to one standard or another, or having the ability to automatically adapt to two or more standards as given by the detected characteristics of the received signal.

While having the most immediate application to cellular telephony at this time, the principles inherent in this invention can be applied by someone skilled in the art to any situation where multiple standards exist for communications.

Since many functions traditionally implemented by dedicated hardware are instead performed via software, the cost, size and power consumption of the resulting terminal is reduced compared to previous art, while the performance and reliability are increased.

We Claim:

1. A self configuring multi-mode communications terminal for adapting to different operating standards comprising:

digital processing circuits, the digital processing circuits further comprising:

a digital signal processor;

first and second memories associated with the digital signal processor;

microprocessor circuits connected to the digital signal processor;

core functionality software stored in the second memory;

at least one set of signal characteristics stored in the second memory, representing at least one standard; and

receiver circuitry connected to the digital signal processing circuits for receiving radio signals, where the receiving circuitry receives and digitizes the radio signal and the core functionality software identifies the standard of the radio signal by comparing the characteristics of the digitized radio signal to the signal characteristics of at least one standard stored in the second memory.

2. The self configuring multi-mode communications terminal for adapting to different operating standards of Claim 1, where the core functionality software downloads, from an available source, a proper executable code for the identified standard into the first memory.

3. The self configuring multi-mode communications terminal for adapting to different operating standards of Claim 2, where the available source is the second memory.

4. The self configuring multi-mode communications terminal for adapting to different operating standards of Claim 2, where the terminal further comprises transmitting circuitry for sending requests for the proper executable code for the identified standard to a remote central network administration system.

5. The self configuring multi-mode communications terminal for adapting to different operating standards of Claim 4, where the receiving circuitry receives the requested proper executable code for the identified standard from the remote central network administration system.

6. The self configuring multi-mode communications terminal for adapting to different operating standards of Claim 5, where the proper executable codes for the identified standard is stored in the second memory.

7. The self configuring multi-mode communications terminal for adapting to different operating standards of Claim 1, where the core functionality software determines the proper executable code by analyzing the digital radio signal.

8. The self configuring multi-mode communications terminal for adapting to different operating standards of Claim 1, where the terminal further comprises transmitting circuitry and where the digital signal processor configures the transmitting circuitry to transmit according to the proper executable code of the identified standard.

9. The self configuring multi-mode communications terminal for adapting to different operating standards of Claim 1, where the core functionality software can be updated to include additional executable code for at least one standard by updating the second memory.

10. The configuring multi-mode communications terminal for adapting to different operating standards of Claim 1, where the core functionality software can be updated to include additional executable code for at least one standard by downloading the additional executable code from a base station, receiving the executable code by the receiving circuitry and storing the executable code in the second memory.

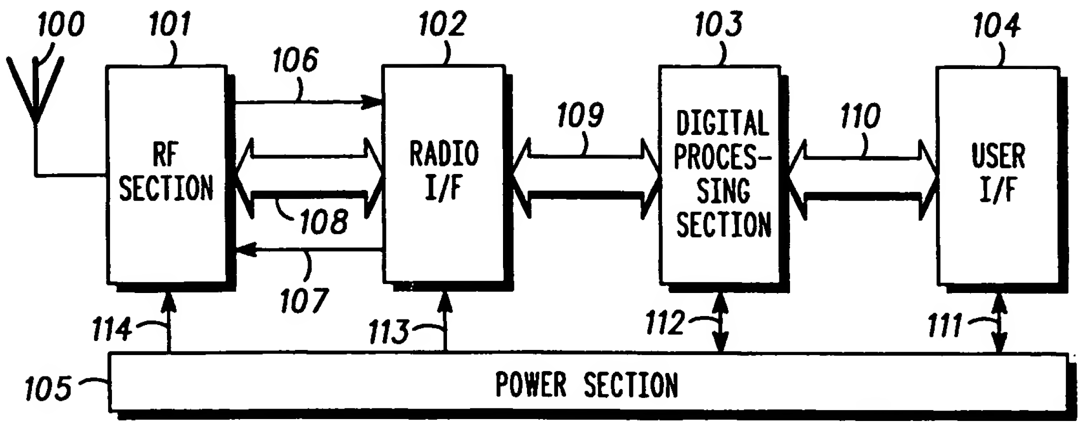
100
101
102
103
104
106
109
110
RF SECTION
RADIO I/F
DIGITAL PROCES-SING SECTION
USER I/F
108
107
114
113
112
111
105
POWER SECTION

FIG.1

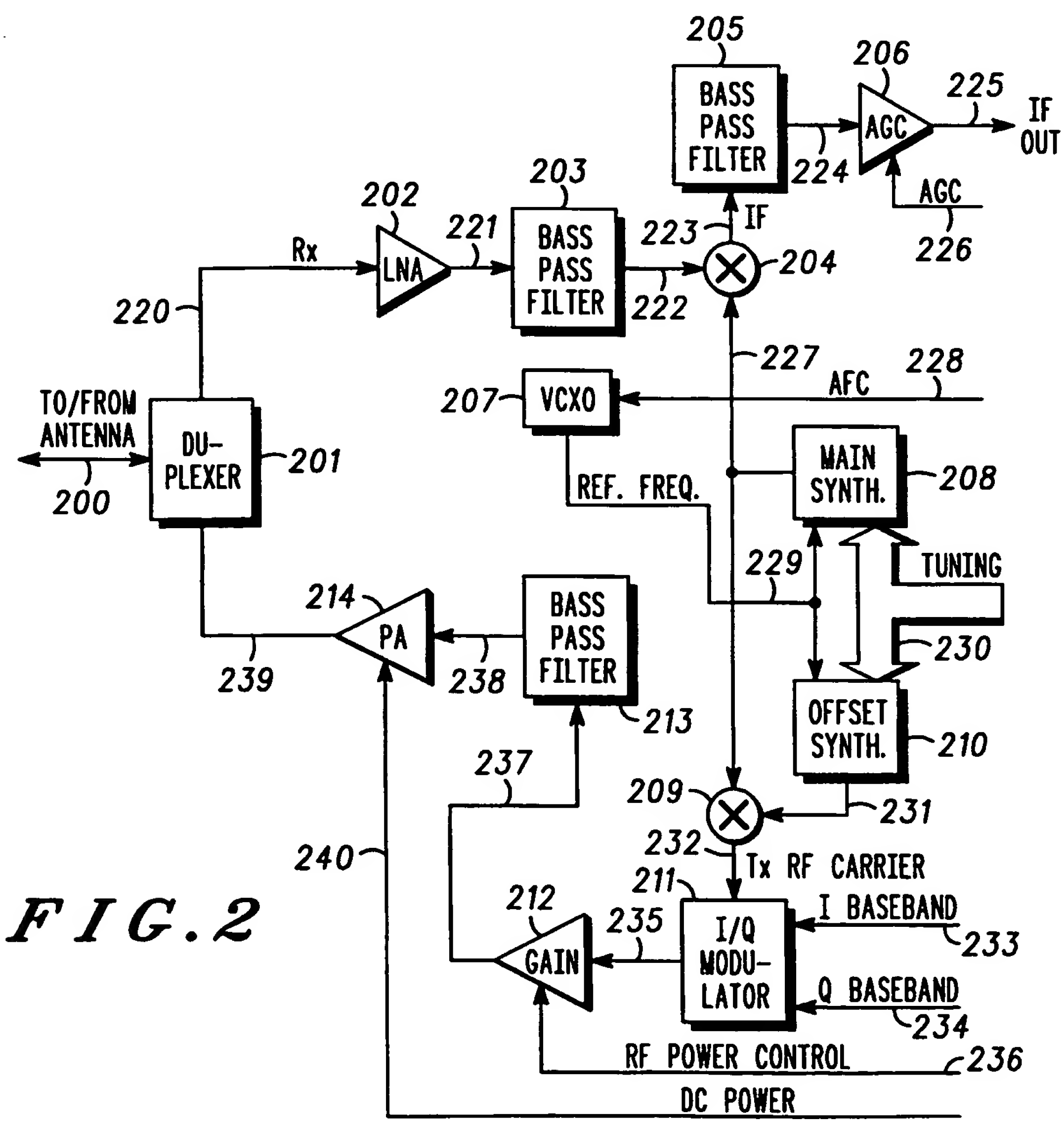
205
206
225
BASS PASS FILTER
AGC
IF OUT
224
AGC
226
203
202
221
223
IF
204
Rx
LNA
BASS PASS FILTER
222
220
227
228
AFC
207
VCXO
TO/FROM ANTENNA
DU-PLEXER
201
MAIN SYNTH.
208
200
REF. FREQ.
229
TUNING
214
BASS PASS FILTER
PA
230
239
238
OFFSET SYNTH.
210
213
237
209
231
240
232
Tx RF CARRIER
211
212
235
I/Q MODU-LATOR
I BASEBAND
233
GAIN
Q BASEBAND
234
RF POWER CONTROL
236
DC POWER

FIG.2

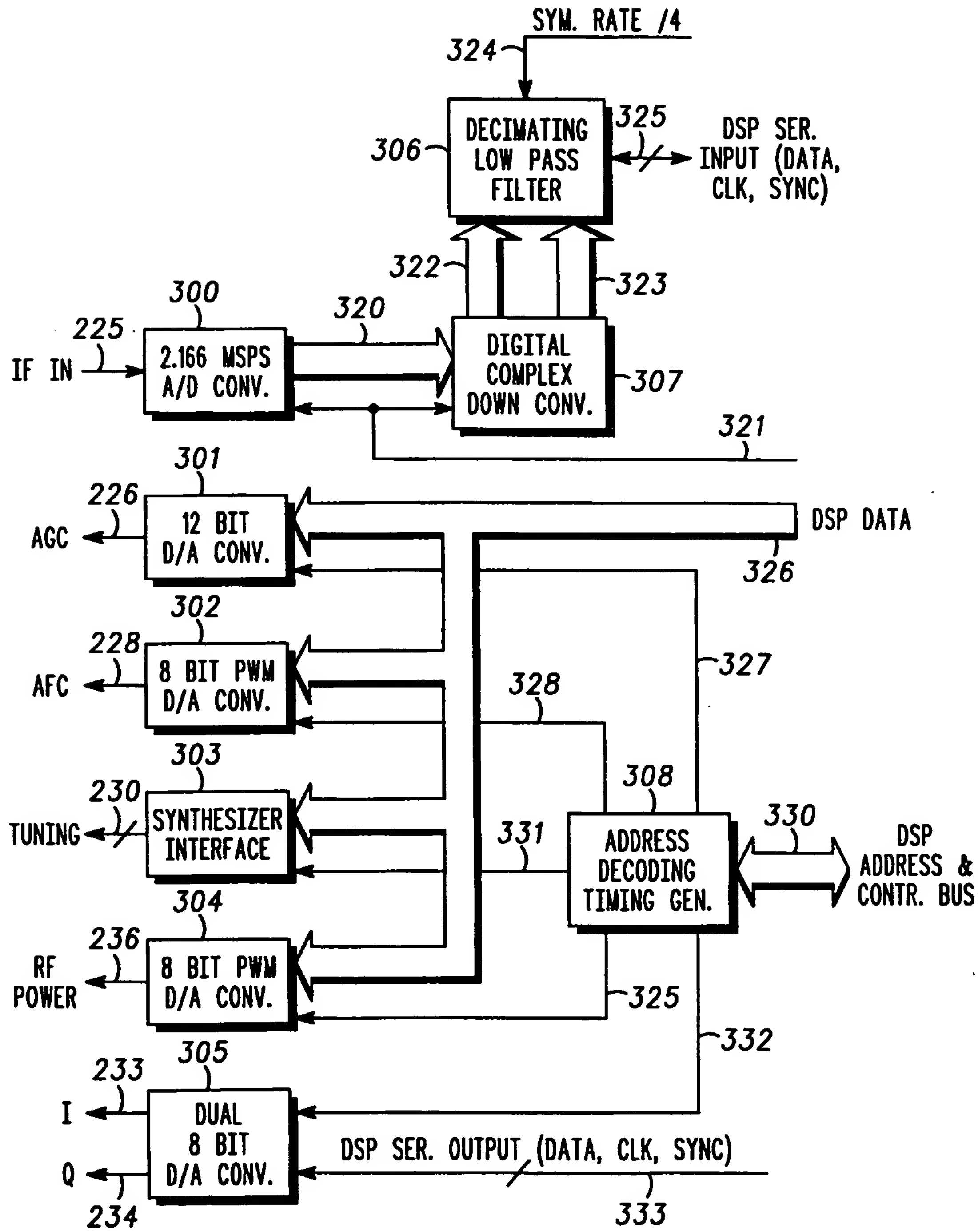
SYM. RATE /4
324
DECIMATING LOW PASS FILTER
306
325
DSP SER. INPUT (DATA, CLK, SYNC)
322
323
300
320
225
IF IN
2.166 MSPS A/D CONV.
DIGITAL COMPLEX DOWN CONV.
307
321
301
226
AGC
12 BIT D/A CONV.
DSP DATA
326
302
228
AFC
8 BIT PWM D/A CONV.
327
328
303
230
TUNING
SYNTHESIZER INTERFACE
308
331
ADDRESS DECODING TIMING GEN.
330
DSP ADDRESS & CONTR. BUS
304
236
RF POWER
8 BIT PWM D/A CONV.
325
332
305
233
I
DUAL 8 BIT D/A CONV.
Q
234
DSP SER. OUTPUT (DATA, CLK, SYNC)
333

FIG.3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/16840

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H04L 27/26; H04B 1/38
US CL :375/216; 455/553
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 375/216, 219-221, 259, 260, 270, 316, 321 ; 455/76, 127, 192.1, 192.2, 234.2, 234.2, 552, 553, 561; 370/330, 436, 455

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS (mode, signal processor, volatile or non-volatile memory, transmitter, and receiver)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 5,745,523 A (DENT ET AL.) 28 APRIL 1998, COL. 3, LINES 40-55, COL. 5, LINES 52-63, AND COL. 6, LINES 22-34.	1-10
X,P	US 5,732,359 A (BARANOWSKY, II ET AL.) 24 MARCH 1998, COL. 6, LINES 48-61 AND COL. 8, LINES 35-49.	1-10
X,P	US 5,691,709 A (GUNTIN) 25 NOVEMBER 1997, COL. 9, LINES 16-35, COL. 10, LINES 39-52, AND COL. 11, LINES 40-56.	1-10
X	US 5,564.092 A (GRANDFIELD ET AL.) 08 OCTOBER 1996, COL. 2, LINE 60 TO COL. 3, LINE 29, COL. 4, LINES 11-16, AND COL. 6, LINES 22-30.	1-10

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 OCTOBER 1998	09 DEC 1998

Name and mailing address of the ISA/US	Authorized officer
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,251,232 A (NONAMI) 05 October 1993, col. 3, lines 34-44.	1-10
A	US 5,404,579 A (OBAYASHI et al.) 04 April 1995, figure 2.	1-10
A	US 5,309,429 A (FUKUDA) 03 May 1994, figure 3.	1-10
A	US 5,020,093 A (PIREH) 28 May 1991, col. 3, lines 37-68.	1-10